# HA :-

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all; entity HA is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

sum : out STD\_LOGIC; carry : out STD\_LOGIC);

end HA;

architecture Behavioral of HA is

begin

sum<= a xor b; carry<= a and b;

end Behavioral;

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# HA test bench: -

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity HA\_tb is

-- Port ( ); end HA\_tb;

architecture Behavioral of HA\_tb is component HA is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

sum : out STD\_LOGIC;

carry : out STD\_LOGIC); end component;

signal a,b,sum,carry:STD\_LOGIC;

begin

U1: HA port map(a,b,sum,carry); process

begin a<='0';

b<='0';

wait for 100ns; a<='0';

b<='1';

wait for 100ns; a<='1';

b<='0';

wait for 100ns; a<='1';

b<='1';

wait for 100ns; end process; end Behavioral; **output :-**

